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1 Collaborative document monitoring

Natalie Glance, Jean-Luc Meunier, Pierre Bernard, Damián Arregui

September 2001 **GROUP '01:** Proceedings of the 2001 International ACM SIGGROUP Conference on Supporting Group Work

Publisher: ACM Request Permissions

Full text available: Pdf (449.24 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 28, Citation Count: 2

In this paper we present a second generation URL monitoring tool which enables the collaborative evaluation of URL content changes. In our implementation, a document monitoring agent works alongside a recommender system. Using information provided by ...

Keywords: URL monitoring agent, WWW, recommender system

2 Modeling layout tools to derive forward estimates of area and delay at the RTL level

Donald S. Gelosh, Dorothy E. Stoliff

July 2000 **Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Publisher: ACM Request Permissions

Full text available: Pdf (278.32 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 38, Citation Count: 0

Forward estimates of area and delay facilitate effective decision-making when searching the solution space of digital designs. Current estimation techniques focus on modeling the layout result and fail to deliver timely or accurate estimates. This paper ...

Keywords: VLSI CAD, estimation, estimation techniques, layout, machine learning

3 Aurora: a new model and architecture for data stream management

Daniel J. Abadi, Don Carney, Ugur Çetintemel, Mitch Cherniack, Christian Convey, Sangdon Lee, Michael Stonebraker, Nesime Tatbul, Stan Zdonik

August 2003 **The VLDB Journal — The International Journal on Very Large Data Bases** , Volume 12 Issue 2

Publisher: Springer-Verlag New York, Inc.

Full text available: Pdf (585.97 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 24, Downloads (12 Months): 185, Citation Count: 103

Abstract.This paper describes the basic processing model and architecture of Aurora, a new system to manage data streams for monitoring applications. Monitoring applications differ substantially from conventional business data processing. The fact that ...

Keywords: Continuous queries, Data stream management, Database triggers, Quality-of-service, Real-time systems

4 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

November 1997 **CASCON '97:** Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research

Publisher: IBM Press

Full text available: Pdf (4.21 MB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 38, Downloads (12 Months): 387, Citation Count: 0

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event ...

5 Efficient circuit clustering for area and power reduction in FPGAs

Amit Singh, Ganapathy Parthasarathy, Malgorzata Marek-Sadowska

October 2002 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 7 Issue 4

Publisher: ACM Request Permissions

Full text available: Pdf (3.26 MB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 17, Downloads (12 Months): 80, Citation Count: 3

We utilize Rent's rule as an empirical measure for efficient clustering and placement of circuits in clustered Field Programmable Gate Arrays (FPGAs). We show that careful matching of resource availability and design complexity during the clustering ...

Keywords: FPGA, Rent, clustering, congestion, interconnect, placement, power

6 Behavioral synthesis of field programmable analog array circuits

Haibo Wang, Sarma B. K. Vrudhula

October 2002 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 7 Issue 4
Publisher: ACM Request Permissions

Full text available: Pdf (519.64 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 42, Citation Count: 2

This article presents methods to translate a behavioral-level analog description into a Field Programmable Analog Array (FPAA) implementation. The methods consist of several steps that are referred to as function decomposition, macrocell synthesis, placement ...

Keywords: Programmable circuits, analog synthesis

7 Low-power high-level synthesis for FPGA architectures

Deming Chen, Jason Cong, Yiping Fan

August 2003 **ISLPED '03:** Proceedings of the 2003 international symposium on Low power electronics and design
Publisher: ACM Request Permissions

Full text available: Pdf (254.82 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 104, Citation Count: 15

This paper addresses two aspects of low-power design for FPGA circuits. First, we present an RT-level power estimator for FPGAs with consideration of wire length. The power estimator closely reflects both dynamic and static power contributed by various ...

Keywords: FPGA power reduction, RT-level power estimation, data path optimization

8 From VHDL to efficient and first-time-right designs: a formal approach

Peter F. A. Middelhoek, Sreeranga P. Rajan

April 1996 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 1 Issue 2
Publisher: ACM Request Permissions

Full text available: Pdf (722.99 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 12, Downloads (12 Months): 78, Citation Count: 2

In this article we provide a practical transformational approach to the synthesis of correct synchronous digital hardware designs from high-level specifications. We do this while taking into account the complete life cycle of a design from early prototype ...

Keywords: CDFG, SFG, VHDL, correctness by construction, design methodology, rapid system prototyping, transformational design

9 Extending Java for high-level Web service construction

Aske Simon Christensen, Anders Møller, Michael I. Schwartzbach

November 2003 **Transactions on Programming Languages and Systems (TOPLAS)** , Volume 25 Issue 6
Publisher: ACM Request Permissions

Full text available: Pdf (947.02 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 18, Downloads (12 Months): 137, Citation Count: 28

We incorporate innovations from the <bigwig> project into the Java language to provide high-level features for Web service programming. The resulting language, JWIG, contains an advanced session model and a flexible mechanism for dynamic construction ...

Keywords: Interactive Web services, XML, data-flow analysis

10 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 1 Issue 1
Publisher: ACM Request Permissions

Full text available: Pdf (550.02 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 62, Downloads (12 Months): 418, Citation Count: 89

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design